CLAIMS

1. A printed circuit board product comprising:
a dielectric structure core having a first surface; and
at least two conducting pads on the first surface of the dielectric structure core, wherein the at least two conducting pads are separated by a pad edge-to-pad edge separation distance of less than 12 mils.

2. The printed circuit board product of claim 1 wherein the pad edge-to-pad edge separation distance of the at least two conducting pads is 3 mils. to 10 mils.

3. The printed circuit board product of claim 2 wherein the pad edge-to-pad edge separation distance of the at least two conducting pads is 8 mils.

4. The printed circuit board product of claim 1 and further including:
a substantially zero signal degradation electrical connection between the at least two conducting pads.

5. The printed circuit board product of claim 4 wherein the substantially zero signal degradation electrical connection is solder.

6. The printed circuit board product of claim 5 wherein the at least two conducting pads includes:
a first conducting pad having an edge; and
a second conducting pad having an edge separated from and adjacent to the edge of the first conducting pad, the edges of the first and second conducting pads defining therebetween a surface area of the first surface, wherein the solder only partially covers the surface area.

7. The printed circuit board product of claim 6 wherein the solder covers substantially all of the surface area.

8. A printed circuit board product comprising:

a dielectric structure core having a first surface;

at least two conducting pads on the first surface of the dielectric structure core; and

a solder bridge electrical connection between the at least two conducting pads.

9. The printed circuit board product of claim 8 wherein the at least two conducting pads includes:

a first conducting pad having an edge; and

a second conducting pad having an edge separated from and adjacent to the edge of the first conducting pad, the edges of the first and second conducting pads defining a surface area of the first surface therebetween, wherein the solder bridge electrical connection only partially covers the surface area.

10. The printed circuit board product of claim 9 wherein the solder bridge electrical connection covers substantially all of the surface area.

11. The printed circuit board product of claim 8 wherein the solder bridge electrical connection is a substantially zero signal degradation electrical connection.

12. The printed circuit board product of claim 8 wherein the solder bridge electrical connection is formed from solder paste.

13. The printed circuit board product of claim 12 wherein the solder paste is applied to the first surface of the dielectric structure core through a stencil.

14. A method of fabricating a substantially zero signal degradation electrical connection on a printed circuit board, the method comprising the steps of:

providing a printed circuit board defined by a dielectric structure core having a first surface, the first surface including a first conducting pad having an edge and a second conducting pad having an edge separated from and adjacent to the edge of the first conducting pad, the edges of the first and second conducting pads defining therebetween a surface area of the first surface;

applying a solder paste on the first and second conducting pads and on the first surface of the dielectric structure core, the solder paste at least partially covering the surface area of the first surface between the edges of the first and second conducting pads to form a substantially zero signal degradation electrical connection between the first and second conducting pads.

15. The method of claim 14, and further including the step of:

performing reflow soldering of the solder paste applied to the first and second conducting pads and the surface area of the first surface of the dielectric structure core.

16. The method of claim 14 wherein the step of applying the solder paste includes the steps of:

placing a stencil on the first surface of the dielectric structure core, the stencil defining a first opening sized to substantially correspond to the first conducting pad, a second opening sized to substantially correspond to the second conducting pad and a third opening that links the first opening to the second opening and is sized to correspond to a partial portion of the surface area of the first surface between the edges of the first and second conducting pads; and

applying the solder paste onto the stencil so that the solder paste flows through the first, second and third openings and onto the first and

second conducting pads and the first surface of the dielectric structure core.

17. The method of claim 16, and further including the steps of:

removing the stencil from the first surface of the dielectric structure core; and

performing reflow soldering of the solder paste applied to the first and second conducting pads and the surface area of the first surface of the dielectric structure core.

18. The method of claim 14 wherein the step of applying the solder paste includes:

applying the solder paste on the first surface of the dielectric structure core such that the solder paste covers substantially all of the surface area of the first surface between the edges of the first and second conducting pads to form a substantially zero signal degradation electrical connection between the first and second conducting pads.

19. The method of claim 18 wherein the step of applying the solder paste includes the steps of:

placing a stencil on the first surface of the dielectric structure core, the stencil defining an opening sized to substantially correspond to the first conducting pad, the second conducting pad and substantially the entire surface area of the first surface between the edges of the first and second conducting pads; and

applying the solder paste onto the stencil so that the solder paste flows through the opening and onto the first and second conducting pads and the first surface of the dielectric structure core.

20. The method of claim 19, and further including the steps of:

removing the stencil from the first surface of the dielectric structure core; and

performing reflow soldering of the solder paste applied to the first and second conducting pads and the surface area of the first surface of the dielectric structure core.

21. The method of claim 19 wherein the stencil includes a plurality of openings in addition to the opening, and wherein prior to the step of placing the stencil on the first surface of the dielectric core the method includes the step of:

masking off at least one opening of the plurality of openings such that the solder paste is prevented from flowing through the at least one opening.

22. The method of claim 14 wherein the edge of the second conducting pad is separated from the edge of the first conducting pad by a pad edge-to-pad edge separation distance of less than 12 mils.

23. The method of claim 22 wherein the pad edge-to-pad edge separation distance is 8 mils.

24. A stencil device for insuring that solder paste is accurately applied to a printed circuit board to create a substantially zero signal degradation solder bridge electrical connection, the printed circuit board being defined by a dielectric structure core having a first surface, the first surface including a first conducting pad having an edge and a second conducting pad having an edge separated from and adjacent to the edge of the first conducting pad, the edges of the first and second conducting pads defining therebetween a surface area of the first surface, the stencil device comprising:

a stencil plate member defining a first opening sized to substantially correspond to the first conducting pad, a second opening sized to substantially correspond to the second conducting pad and a third opening that links the first opening to the second opening and is

sized to correspond to a partial portion of the surface area of the first surface between the edges of the first and second conducting pads, such that upon application of solder paste to the stencil plate member, the solder paste flows through the first, second and third openings onto the first and second conducting pads and the first surface of the dielectric structure core to form a substantially zero signal degradation electrical connection between the first and second conducting pads.

25. A stencil device for insuring that solder paste is accurately applied to a printed circuit board to create a substantially zero signal degradation solder bridge electrical connection, the printed circuit board being defined by a dielectric structure core having a first surface, the first surface including a first conducting pad having an edge and a second conducting pad having an edge separated from and adjacent to the edge of the first conducting pad, the edges of the first and second conducting pads defining therebetween a surface area of the first surface, the stencil device comprising:

a stencil plate member defining an opening sized to substantially correspond to the first conducting pad, the second conducting pad and substantially the entire surface area of the first surface between the edges of the first and second conducting pads, such that upon application of solder paste to the stencil plate member, the solder paste flows through the opening onto the first and second conducting pads and the first surface of the dielectric structure core to form a substantially zero signal degradation electrical connection between the first and second conducting pads.